P

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10053543	01/24/2002	~~257~~ 438	200 +	2814	PERALTA

**APPLICANTS: Shimizu Masahiro; Tanaka Yoshinori; Arima Hideaki;

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 09/452,099 12/02/1999

WHICH IS A DIV OF 09/119,053 07/20/1998 PAT 6,066,861

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 10-017232(P) 01/29/1998

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		
Verified and Acknowledged Examiners's intials			57454-329

TITLE : Integrated circuit having a memory cell transistor with a gate oxide layer which is thicker than the gate oxide layer of a peripheral circuit transistor

U S DEPT. OF COMM./PAT & TM-PTO-436L/Rev 12-94

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM

(Attached in pocket on right inside flap)